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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,714	12/20/2000	Mohamed S. El-Hennawey	91436-283CIP	3264

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EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,714	EL-HENNAWEY ET AL.	
	Examiner	Art Unit	
	Syed J. Ali	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed October 25, 2004. Claims 1-14 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Specification

3. The cross reference related to the application cited in the specification must be updated (i.e. update the relevant status, with PTO serial numbers or patent numbers where appropriate, on page 1, lines 7-10). The entire specification should be so revised.

Claim Rejections - 35 USC § 102

4. **Claims 1 and 4-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu (USPN 6,104,721).**

5. As per claim 1, Hsu teaches the invention as claimed, including a method of processing communication channels, comprising:

for each of a plurality of channels:

undertaking a given channel processing task for a given channel with one processor of a plurality of processors, said one processor optimized for said given channel processing task (col. 6 lines 43-46; col. 7 lines 8-20; col. 10 lines 37-53);

storing instance data for said given channel processing task in a memory which may be associated with any one of said plurality of processors such that said instance data is associated with said one processor (col. 7 lines 23-33; col. 8 lines 27-40);

when said given channel processing task for said given channel changes to a new channel processing task for which said one processor is not optimized,

moving processing of said given channel to a different one of said plurality of processors, said different one of said plurality of processors being optimized for said new channel processing task (col. 9 lines 24-40; col. 10 lines 3-10; col. 10 lines 48-53), and

changing association of said stored given channel instance data to an association with said different one of said plurality of processors (col. 8 lines 27-40; col. 10 lines 3-10).

6. As per claim 4, Hsu teaches the invention as claimed, including the method of claim 1 wherein said moving comprises consulting a table for a processor optimized to said new channel processing task (col. 6 line 65 - col. 7 line 2; col. 10 lines 3-10).

7. As per claim 5, Hsu teaches the invention as claimed, including the method of claim 1 wherein said memory is a multiplexed memory (col. 7 lines 23-33; col. 7 lines 49-64; col. 8 lines 27-40).

8. As per claim 6, Hsu teaches the invention as claimed, including the method of claim 1 further comprising, where said one processor is optimized for said new channel processing task,

undertaking said new channel processing task for said given channel at said one processor (col. 9 lines 24-40; col. 10 lines 3-10; col. 10 lines 37-53).

9. As per claim 7, Hsu teaches the invention as claimed, including the method of claim 6 further comprising keeping a table with an identification of available ones of said plurality of processors and an identification of processing tasks handled by said available ones of said plurality of processors (col. 6 line 65 - col. 7 line 2; col. 10 lines 3-10).

10. As per claim 8, Hsu teaches the invention as claimed, including the method of claim 5 wherein said changing association comprises overwriting a latch holding an address of said one processor with an address of said different one of said plurality of processors (col. 10 lines 3-10).

11. As per claim 9, Hsu teaches the invention as claimed, including a method of processing communication channels comprising:

at each of a plurality of processors:

undertaking a channel processing task using a multiplexed memory having a plurality of channel memory partitions, each of the plurality of channel memory partition for storing channel instance data for a given channel (col. 6 lines 43-46; col. 7 lines 8-20; col. 7 lines 49-64; col. 10 lines 37-53);

when said channel processing task changes to a new channel processing task (col. 13 lines 6-42):

referencing a table to identify a new task optimized processor of said plurality of processors optimized to said new channel processing task (col. 6 line 65 - col. 7 line 2; col. 10 lines 3-10),

prompting said new task optimized processor to assume processing of said given channel (col. 6 line 65 - col. 7 line 2; col. 10 lines 3-10), and

arranging for an associator to associate channel instance data stored in one of said plurality of channel memory partitions and associated with said given channel with said new task optimized processor (col. 10 lines 3-10).

12. As per claim 10, Hsu teaches the invention as claimed, including a multiprocessor system for processing communications channels, comprising:

a plurality of processors, each optimized for at least one channel processing task and each having processor memory for storing information associating different channel processing tasks to different ones of said processors (col. 6 lines 43-46; col. 7 lines 8-20; col. 10 lines 37-53);

a multiplexed memory for storing channel processing instance data for each of said plurality of processors (col. 7 lines 23-33; col. 7 lines 49-64; col. 8 lines 27-40);

an associator for associating channel processing instance data for each channel with one of said plurality of processors (col. 7 lines 49-64; col. 10 lines 3-10);

each processor of said plurality of processors operable to, on a channel processing task for a channel currently being processed by said each processor changing to a new task,

arrange for said associator to associate instance data for said channel with a processor optimized to said new task (col. 7 lines 49-64; col. 10 lines 3-10).

13. As per claim 11, Hsu teaches the invention as claimed, including the system of claim 10 further comprising a host for, on a channel processing task for a channel currently being processed by a given processor changing to a new task, sending to said given processor an indication of said processor optimized to said new task (col. 14 lines 51-62).

14. As per claim 12, Hsu teaches the invention as claimed, including the system of claim 10 wherein said associator comprises a latch for channel instance data of a given channel, each said latch being latched to a given processor processing said given channel and arranged such that only said given processor may change said latch to a new processor (col. 10 lines 3-10).

15. As per claim 13, Hsu teaches the invention as claimed, including the system of claim 12 wherein said associator further comprises a multiplexer mapping memory read/write requests from said given processor to instance channel data for said given channel in said shared memory (col. 9 lines 24-40; col. 10 lines 3-10; col. 10 lines 48-53).

16. As per claim 14, Hsu teaches the invention as claimed, including the system of claim 13 wherein each of said plurality of processors is a digital signal processor ["DSP"] (col. 1 lines 16-22).

Claim Rejections - 35 USC § 103

17. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Weiss et al. (USPN 5,526,363) (hereinafter Weiss).**

18. As per claim 2, Weiss teaches the invention as claimed, including the method of claim 1 wherein said stored given channel instance data comprises a history buffer storing historical data samples for a signal on said given channel (col. 3 lines 30-58).

19. It would have been obvious to one of ordinary skill in the art to combine Hsu and Weiss since predictive assignment of processing channels to processors would be enabled, thereby increasing the efficiency of the system by utilizing a processor that is best suited to process a particular signal.

20. **Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Lin et al. (USPN 6,606,306) (hereinafter Lin).**

21. As per claim 3, Lin teaches the invention as claimed, including the method of claim 1 wherein said stored given channel instance data comprises a jitter buffer (col. 3 line 66 - col. 4 line 19).

22. It would have been obvious to one of ordinary skill in the art to combine Hsu and since the use of a jitter buffer would enable smoother processing of audio and visual signals, thereby improving the quality of the signal processing.

Response to Arguments

23. **Applicant's arguments filed April 21, 2005 have been fully considered but they are not persuasive.**

24. Applicant argues that "*Hsu does not teach optimization as recited in the independent claims.*" Applicant points out that the meaning of "optimized" is set forth on page 6 of the specification, i.e. DSP cores are optimized to handle specific channel processing tasks by downloading software from a shared memory to the memory of the DSP core.

25. Hsu teaches the plurality of DSPs each being configured to perform various types of tasks by loading their local memory with particular operational codes (col. 7 lines 26-29, "Each of local memory spaces...stores DSP operational codes, as explained further below, for operating the corresponding processor"). Thus, each DSP is "optimized" to run certain types of tasks based upon the operational codes provided to it. The resource controller then distributes tasks to an "optimized" DSP depending on what type of tasks the various DSPs are "optimized" to perform (col. 9 lines 48-56, "Service definition field 174 is used to store information representative of all service types currently supported by the DSP operational code of the corresponding processor. Each processor of processing bank 112...provides this information to the resource controller 114. Call assignments are performed by the resource controller based on this information").

26. Applicant argues that "*Hsu does not teach...moving processing between processors as recited in the independent claims.*" To support this argument, Applicant argues that "*once the*

[processor] assignment is made, there is no indication that the channel is moved to another processor as recited in the claim." On page 6 of Applicant's specification, it is indicated that the channel is moved from one processor to another by referencing a table and resetting a memory partition such that it is associated with a new processor that is capable of performing the processing.

27. First, it should be noted that "moving processing", as claimed, does not indicate that a processor performing processing of a particular task offloads the task to another processor. Rather, new tasks arriving on the channel are assigned to a different processor that is capable of performing the type of processing. This is supported by Applicant's specification, which indicates that the memory partition is altered such that incoming data on a channel is assigned to a different processor. Contrary to Applicant's assertion that Hsu does not teach this feature is the fact that Hsu teaches dynamic resource allocation, such that when a new task arrives at the resource controller, a determination is made as to whether the currently assigned DSP is appropriate, and reassigning the channel if it is not (col. 13 lines 6-42, "the controller selects the proper processor or plurality of processors from processing bank 112...to service the incoming call", "the resource controller updates the status of the MRC table...by, for example, revising the status of the channel assignment status field").

28. Applicant argues that the limitation of claim 9 reading "when said channel processing task changes to a new channel processing task" has not been addressed. This limitation is preliminary in nature and merely provides the circumstance in which the subsequent events take

place. The limitation in itself performs no function. Nonetheless, Examiner has indicated where this "element" of the claim can be found in Hsu.

29. Applicant argues that there is no motivation to combine Hsu and Weiss since "*the asserted motivation lacks the evidence required by the Federal Circuit.*" Applicant submits that the articulated motivation must be supported by actual evidence before an obviousness determination can be made. Applicant makes a similar argument with respect to the combination of Hsu and Lin.

30. Examiner has provided evidence of the knowledge of one of ordinary skill in the art, which has been held as being sufficient to support an obviousness motivation. *In Re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). With respect to the combination of Hsu and Weiss, the use of history buffers to generate more likely matches of channel data and DSPs is a well known feature of the prior art. Weiss seeks to improve upon the prior art use of history buffers by creating a shared data structure. It hardly seems appropriate to reconstruct the entire development of the technology of DSPs in order to support an obviousness motivation when the level of ordinary skill in the art is apparent from the Weiss reference itself. The same can be said about the combination of Hsu and Lin. The use of jitter buffers is hardly a new concept, and one of ordinary skill in the art would be well aware that they are frequently used to ensure data is received in a proper order, to smooth signals, or prevent loss of data. In systems with a constant stream of incoming data, the potential for errors is high, so the use of a jitter buffer would provide more reliable data.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
June 8, 2005

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